

GATE-LEVEL SIMULATION OF LOGICAL STATE PREPARATION

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Quantum error correction and fault-tolerant quantum computation are two fundamental concepts which make quantum computing feasible. While providing a theoretical means with which to ensure the arbitrary accuracy of any quantum circuit, fault-tolerant error correction is predicated upon the robust preparation of logical states. An optimal direct circuit and a more complex fault-tolerant circuit for the preparation of the $[[7,1,3]]$ Steane logical-zero are simulated in the presence of discrete quantum errors to quantify the regime within which fault-tolerant preparation of logical states is preferred.

Keywords: quantum error correction, fault-tolerant quantum computation, quantum simulation.

1 Introduction

Faced with the difficulty inherent to the simulation of quantum mechanical systems using classical computers, it was Feynman who first suggested using quantum mechanics itself as a basis for computation [1]. While this idea was formalised by Deutsch, who conceived the universal quantum computer as one which would facilitate the efficient simulation of an arbitrary physical system [2], algorithms developed by Simon [3] and Shor [4] more explicitly demonstrated the potential of the quantum computer, precipitating a number of initial proposals aimed at the physical construction of a working device [5, 6, 7, 8, 9, 10].

Despite this progress, one significant problem which remains an impediment to the realisation of any form of quantum computing is that of quantum errors, which can result from both environmental decoherence and systematic imprecision. Quantum error correction (QEC), devised independently by Shor [11] and by Steane [12] and later generalised by Calderbank and Shor [13] and Steane [14], initially established a means of negating errors afflicting a static qubit. Subsequently, the theory of fault-tolerant quantum computation demonstrated that, by controlling the propagation of errors, QEC

can be undertaken dynamically and in spite of faulty circuit components or externally induced errors [15, 16, 17]. In promising increasingly accurate operation with each level of concatenation, provided that the underlying physical error rate is below some threshold, p_{th} , fault-tolerant quantum computation quickly became the theoretical basis of conventional quantum computing.

Given its importance, a large body of research has endeavored to quantify the threshold error rate for fault-tolerant quantum computation. While this work has comprised some analytic results [18, 19, 16, 20], classical simulation has shown also to be an effective method of threshold estimation. One approach is to simulate the propagation of errors throughout a circuit, rather than the evolution of the entire system state [21]. Several papers have adopted this method for the purposes of threshold estimation [22, 23] and in the evaluation of various ancilla preparation schemes [24, 25]. Correction circuits based upon the stabilizer formalism [16] are particularly conducive to simulation using a package such as CHP (CNOT-Hadamard-Phase) [26], though such a method is not applicable to non-stabilizer codes or true quantum algorithms as the simulation of any stabilizer circuit can be performed efficiently on a classical computer [27]. Other authors have demonstrated the effectiveness of a state vector approach in simulating quantum circuits [28, 29]. However, as errors are modeled by the stochastic application of appropriate gates, the time required to generate statistically significant results becomes prohibitive in the low p regime. As an alternative, the density matrix formalism explicitly includes the stochastic averaging of quantum errors. The limiting factor then becomes the amount of physical memory available to store and manipulate the system density matrix. This approach of gate-level simulation forms the foundation for this research, and is also the basis for other general purpose quantum computer simulators including QuIDD (Quantum Information Decision Diagrams) [30, 31, 32], and is applicable to the simulation of algorithms such as Shor's [33].

Despite the theoretical potential of fault-tolerance to reduce arbitrarily the effect of induced errors, fault-tolerant error correction is predicated upon the encoding of physical qubits to form logical states. Unlike logical gate operation, error correction cannot be undertaken until a complete logical state is encoded. That is, correction cannot be performed after every time step of a preparation circuit. Concatenation further strengthens the requirement of robust logical preparation, as the number of required logical states grows exponentially with each level of recursive encoding. In addition, ancilla networks have been proposed which require logical states as the central resource [34]. While an encoding circuit can itself adhere to the conditions of fault-tolerance, insisting upon fault-tolerant operation will necessarily increase both the number of qubits and the number of gate operations required. This increase in circuit area corresponds directly to an increased logical region within which an error can occur. In contrast, encoding undertaken directly, while not being strictly fault-tolerant, will be vastly simpler in its implementation and will, therefore, be more rapid and less susceptible to the initial occurrence of quantum errors. In practice, and prior to any concatenation, this balance between circuit complexity and the degree of effective error protection implies a crossover error rate, p_{cr} , at which the direct and fault-tolerant implementations of an arbitrary circuit become effectively equivalent. This paper involves the gate-level simulation of direct and fault-tolerant circuits for the preparation of the $[[7,1,3]]$ Steane logical-zero to provide a quantitative determination of the crossover error rate, below which fault-tolerant quantum computation becomes the preferred method of ensuring accurate state preparation.

The structure of this paper is as follows. Sections 2 and 3 comprise a brief overview of the relevant principles underlying both the Steane code and the circuits for logical state preparation. Section 4 details the error model and other technical issues relating to simulation. Results are tabled in Section 5, whereupon the crossover physical error rate is presented.

2 The Steane code

Though the five qubit code [35, 36] represents the most compact QEC protocol, the seven qubit Steane code [12, 14] can be considered a more practical code as universal fault-tolerant computation can be performed more simply [16]. The Steane code is a sufficient protocol to successfully protect against an arbitrary single qubit error, and even multiple errors with non-zero probability of success [37]. The encoding procedure for the Steane code consists of the transformation $\alpha|0\rangle + \beta|1\rangle \rightarrow \alpha|0_L\rangle + \beta|1_L\rangle$, where the logical codewords, $|0_L\rangle$ and $|1_L\rangle$, each comprise a weighted eight-state superposition, and are given by

$$|0_L\rangle = \frac{1}{\sqrt{8}} [|0000000\rangle + |1010101\rangle + |0110011\rangle + |1100110\rangle + |0001111\rangle + |1011010\rangle + |0111100\rangle + |1101001\rangle] \quad (1)$$

$$|1_L\rangle = \frac{1}{\sqrt{8}} [|1111111\rangle + |0101010\rangle + |1001100\rangle + |0011001\rangle + |1110000\rangle + |0100101\rangle + |1000011\rangle + |0010110\rangle]. \quad (2)$$

3 Logical state preparation

The preparation of logical states is a prerequisite for QEC and forms a basis for the proceeding comparison of non fault-tolerant and fault-tolerant quantum computation. Figure 1 outlines the direct circuit for the preparation of the Steane seven qubit logical-zero. For brevity, the corresponding fault-tolerant circuit is omitted from this paper, but is detailed elsewhere [38]. In the formulation of these circuits it is assumed that non-local interaction between qubits is permitted and that isolated two-qubit interactions can be performed simultaneously.

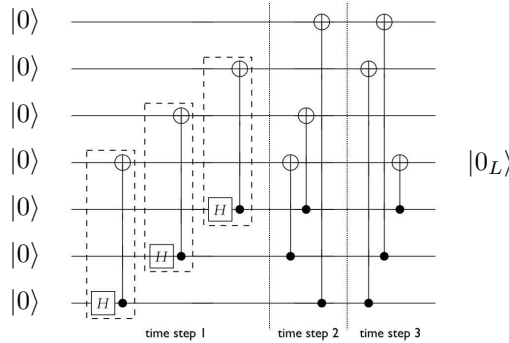


Fig. 1. The direct circuit for seven qubit logical-zero preparation, where dashed boxes represent gates which can, in principle, be compounded via canonical decomposition [39, 40, 41].

The direct implementation comprises a sequence of three time steps, shown explicitly in Figure 1, where combined gates are constructed via canonical decomposition [39, 40, 41]. In the more complex fault-tolerant circuit logical preparation is achieved by the operator measurement of the stabilizers of the Steane logical codewords [15, 16]. However, to maintain fault-tolerance during preparation, each data qubit must interact with a unique ancilla qubit. Therefore, preceding each operator measurement,

a separate ancilla block is initialised and verified, whereupon any deviation from the desired ancilla state will ideally result in the ancilla being reset and the initialisation repeated. A number of protocols exist for the preparation of an appropriate ancilla network, including those optimised for accuracy [25, 34] and those making use of quantum teleportation [42]. To minimise classical memory requirements, Shor’s ancilla [17, 18] is chosen, in which a four qubit ancilla is initialised to the maximally entangled state $\frac{1}{\sqrt{2}}(|0000\rangle + |1111\rangle)$. A fifth ancilla qubit is used to verify the fidelity of this ancilla state prior to each syndrome measurement. To protect against Z errors propagating to the ancilla block, each stabilizer operator is measured multiple times, after which a majority result is taken to specify the syndrome. The significant resource overhead associated with fault-tolerant computation is quantified in the following table contrasting direct and fault-tolerant logical state preparation.

circuit	number of qubits	circuit depth	circuit area	number of gate operations
direct	7	3	21	9
fault-tolerant	12	≥ 60	≥ 720	≥ 108

4 Classical simulation

Classical simulation of the preceding circuits involves storage of the system density matrix, ρ , where gate-level manipulation of the system is achieved through the application of appropriate unitary operations. For a two-level, N particle quantum system the representative density matrix is of dimensionality 2^N , hence a significant memory overhead is associated with even a small number of qubits. Classical simulation is made possible via the implementation of a sparse matrix storage protocol, whereby the density matrix is recast in a tree-like structure with computational memory only being allocated to non-zero matrix elements. To generate this structure the density matrix is divided successively into quadrants, where each quadrant notionally forms a tree branch. Branch subdivision will only continue if a quadrant contains any non-zero elements, otherwise the branch is truncated. Consequently, storage of only the non-zero matrix elements is required, along with their address within the matrix.

Quantum errors are assumed to be stochastic and uncorrelated, such that, at any given time, a discrete error is induced at any location within a circuit with a probability p . Errors are applied to qubits involved in gate operations and also to idle qubits, such that errors occur with equal probability on every qubit after every time step within the circuit. Additionally, each error within the set $\{X, Z, XZ\}$ is assumed to occur with an equal probability given by $p/3$. Following the operator-sum formalism [38, 43], the transformation used in the simulation of quantum errors is given by

$$\rho \longrightarrow \rho' = (1 - p)\rho + \frac{p}{3} (X\rho X^\dagger + Y\rho Y^\dagger + Z\rho Z^\dagger). \quad (3)$$

Given a knowledge of the correctable error set $\{X, Z, XZ\}$, a set of permissible states is known, each of which can be rectified to yield the exact logical-zero. To determine the fidelity of each simulated circuit its output is measured against this set, which comprises the exact logical-zero, where no error has occurred, plus a further 63 states which differ from this state by either a single X error (7), a single Z error (7), or a combination of a single X error and a single Z error applied to arbitrary qubits (49). Logical preparation is defined to be successful if any one of these 64 states is generated, a definition which implicitly assumes that computation can continue following the appropriate correction circuit.

Labeling as ρ_i the density matrices representing each of these correctable states, for a given output, ρ_s , the fidelity of the circuit is defined by

$$|\sum_i \text{tr}(\rho_s \rho_i)|^2. \quad (4)$$

Finally, provisions are made when simulating the fault-tolerant circuit to account for the possibility that ancilla preparation may be repeated and that syndrome measurements may occur two or three times. This dynamic circuit structure is modeled by a list of classical measurement scenarios, each described by a binary string. At each measurement gate in the circuit, a digit in the string is used to force the measurement outcome. By tracking the probability of obtaining the measured outcome at each gate, the overall probability of a particular scenario eventuating can be determined. Scenarios of decreasing likelihood are simulated in this way, with the fidelity of each scenario weighted by its corresponding probability to form an overall circuit fidelity.

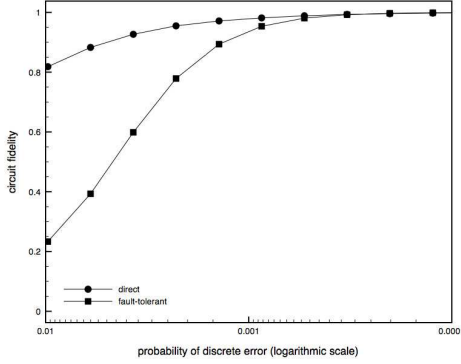
5 Results

Simulations were initially undertaken to determine the susceptibility of the direct implementation to specific single qubit errors. Consistent with the error model, single qubit errors were manually applied after each of the three time steps. As expected, errors were observed to propagate within the circuit to afflict multiple qubits, though these accumulated errors did not invariably lead to circuit failure. Rather, only six errors were observed to generate more than one effective error at the output. For every other error, the cumulative effect of any propagated errors was equivalent to that of only a single error, though not necessarily on the same qubit as was the initial error. This reduction in the effective area of the circuit was attributed to symmetries inherent the code structure. For low p , where the probability of two errors occurring is negligible, the circuit fidelity was analytically calculated as $1 - 4p + O(p^2)$. This result was in complete agreement with simulated results and provided a non-trivial test of the method of simulation.

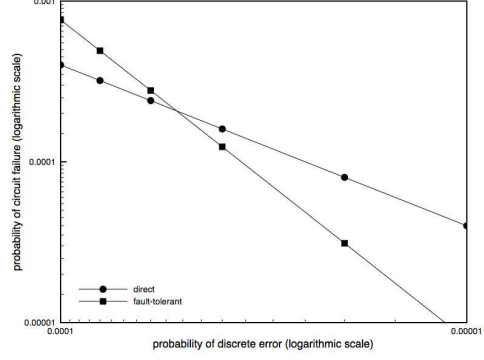
The fidelities of the both the direct and fault-tolerant circuits for logical-zero preparation were evaluated for varying values of the physical error rate p . Results confirmed the relative stability of the direct circuit in the high p regime, as is illustrated in Figure 2(a). In this region, the significant complexity introduced in the fault-tolerant circuit increases dramatically the probability that multiple errors will occur. For lower values of p , it was expected that the fault-tolerant circuit would fail with probability cp^2 , where c is the number of pairs of locations at which two errors can occur. By convention, a naive estimate of c can be made by considering the circuit area A , such that

$$c \approx \binom{A}{2} \geq \binom{720}{2} = 2.6 \times 10^5. \quad (5)$$

The fault-tolerant circuit was found to be more robust than predicted by this simple estimation. Based upon the simulated data, c was determined to equal approximately 7.7×10^4 , implying that the fault-tolerant circuit does not fail upon the application of every two error combination. While the observed reduction in the effective area of the fault-tolerant circuit is partly analogous in both cause and effect to that observed of the direct circuit, this reduction can also be attributed to the fault-tolerant structure of both ancilla preparation and syndrome extraction. For example, as certain errors during preparation can be detected, these errors will not contribute to the set of errors which cause circuit failure.



(a) Fidelity of the direct and fault-tolerant circuits for logical-zero preparation in the presence of quantum errors. Results shown span the high p regime, in which the direct circuit is relatively robust.



(b) The crossover error rate at which fault-tolerant and direct preparation become effectively equivalent. For physical error rates below 5.3×10^{-5} the fault-tolerant circuit achieves logical state preparation with a greater reliability than the equivalent direct implementation

Fig. 2.

This general result further serves to illustrate a significant advantage of gate-level simulation, as it facilitates a direct observation of the response of a complex circuit to quantum errors. Moreover, the quantitative analysis of error combinations has been tied previously to a rigorous determination of the fault-tolerant threshold [44].

The crossover physical error rate at which the direct and fault-tolerant circuits operated with equal fidelity was observed at $p_{cr} \approx 5.3 \times 10^{-5}$. Figure 2(b) illustrates the crossover and highlights the behaviour of each circuit in the low p regime. As expected, in this region the direct circuit fails with probability $O(p)$, while the corresponding fault-tolerant circuit fails with probability $O(p^2)$. Assuming that a quantum computer will operate with an error rate of approximately p_{cr} then implies that fault-tolerant preparation may enable logical encoding of data with a higher fidelity than direct preparation. In contrast, the compact nature of the direct circuit will allow more logical states to be prepared for use as ancillas in a given cycle of QEC. Recent research has demonstrated that non-fault tolerant ancilla preparation, coupled either with a verification procedure [45] or with a decoding procedure [46], is important in achieving an attractive threshold when considering an ancilla network with logical states as the primary resource.

6 Conclusion

A crossover physical error rate was observed at approximately 5.3×10^{-5} , below which the fault-tolerant implementation becomes the preferred method of state preparation. The complexity associated with the fault-tolerant circuit clearly provides the major impediment to its stability under quantum errors. Though fault-tolerant preparation is, at present, unable to operate effectively in the region of realistic physical error rates, fault-tolerant computation is necessary to achieving the increased fidelity afforded by concatenated QEC. Thus, while higher order QEC codes may prove to be more

robust, more rapid and efficient fault-tolerant circuits must be designed that take advantage of non fault-tolerant components where appropriate such that maximum stability is achieved. This process should be aided by the simulation of other direct and fault-tolerant circuits, including correction and transversal gate operation.

In undertaking further simulation, greater consideration must be given to the environment in which quantum computation will inevitably take place. To this effect, recent threshold analyses have been undertaken in the context of a specific spatial arrangement of qubits [47, 45]. In addition, while the model described in Section 4 is common within QEC analyses, and in spite of previous research investigating the effects of local non-Markovian noise on computation [48, 44], a more thorough error model should more accurately reflect the physical properties of a specific computing architecture. For example, a given architecture may be more vulnerable to dephasing errors, or may experience high rates of qubit loss. Errors may also be attributed to inaccurate gate implementation, in which the assumption of non-correlated error effects will be invalidated, and errors associated with qubit transport must accompany any analysis of concatenated architectures, which are vital to any practical realisation of the threshold theorem. Such spatial and physical considerations not only highlight the challenge of accurately and realistically simulating quantum circuits, but demonstrate explicitly the need for circuits conceived in the context of specific physical architectures.

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